

# Arria 10 SoC Low Profile PCIe FPGA Board

System-on-Chip FPGA with dual QSFPs and DDR4

The 385A-SoC™ low profile accelerator card provides a powerful computing and I/O platform for FPGA and ARM-based development and deployment across a range of application areas including high performance computing, image processing, and network analytics.

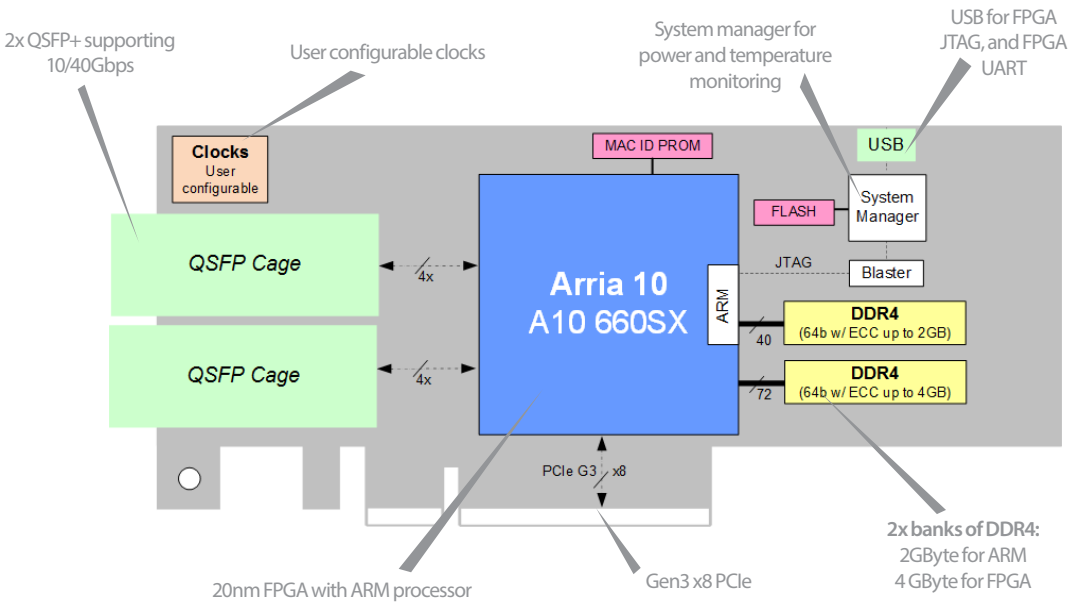
**Key Applications**

Designed to address a range of compute-intensive and latency-critical applications, including:

- Machine Learning Inference
- Internet of Things
- Intelligent Storage Gateway
- Real-time Network Analytics

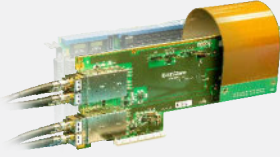
## key features

- Intel Arria 10 SoC SX 660
- 2x QSFP+ for 10/40Gbps
- Embedded BSP (ARM)



# Additional Services

Take advantage of BittWare's range of design, integration, and support options



## Customization

[Additional specification options](#) or [accessory boards](#) to meet your exact needs.



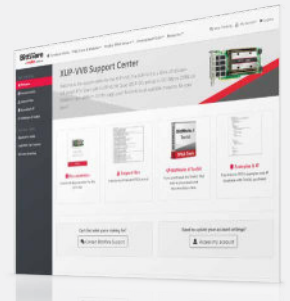
## Server Integration

Available pre-integrated in our [TeraBox servers](#) in a range of configurations.



## Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



## Service and Support

BittWare Developer Site provides online documentation and issue tracking.

## Board Specifications

FPGA	<ul style="list-style-type: none"> <li>Intel Arria 10 SX               <ul style="list-style-type: none"> <li>660 SX in F34 package</li> <li>Core speed grade -2</li> </ul> </li> </ul>
On-board Flash	<ul style="list-style-type: none"> <li>Flash memory for booting FPGA</li> </ul>
On-board memory	<ul style="list-style-type: none"> <li>One bank of DDR4 SDRAM x 72 for FPGA fabric, 4GB @ 2133MT/s</li> <li>One bank of DDR4 SDRAM x 40 for ARM processor, 2GB @ 2133MT/s</li> </ul>
Host interface	<ul style="list-style-type: none"> <li>x8 Gen3 interface direct to FPGA</li> </ul>
QSFP cages	<ul style="list-style-type: none"> <li>2 QSFP+ cages on front panel connected directly to FPGA via 8 transceivers</li> <li>User programmable low jitter clocking supporting 10/40 GbE</li> <li>Each QSFP can be independently clocked</li> <li>Clocking options:               <ul style="list-style-type: none"> <li>Network recovered with jitter attenuation</li> <li>QSFP clocking: user programmable, or CPRI, 1GbE</li> <li>External clock input, 1PPS input</li> </ul> </li> </ul>
Power supply monitoring and reporting	<ul style="list-style-type: none"> <li>On-board Altera USB Blaster</li> <li>Voltage monitoring</li> <li>Temperature monitoring</li> <li>Fault condition reporting to FPGA</li> </ul>
Cooling	<ul style="list-style-type: none"> <li>Standard: single-width active heatsink (embedded fan)</li> <li>Optional: single-width passive heatsink</li> </ul>

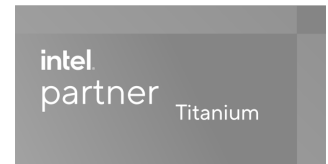
Electrical	<ul style="list-style-type: none"> <li>On-board power derived from 12V PCIe slot</li> <li>Power dissipation is application dependent</li> </ul>
Environmental	<ul style="list-style-type: none"> <li>Operating temperature: 5°C to 35°C</li> </ul>
Quality	<ul style="list-style-type: none"> <li>Manufactured to IPC-A-610 Class 2</li> <li>RoHS compliant</li> </ul>
Form factor	<ul style="list-style-type: none"> <li>Half-height, half-length PCIe single-slot board</li> <li>2.713 x 6.6 inches (68.9 x 167.6 mm)</li> </ul>

## Development Tools

FPGA development	<b>BIST</b> - Built-In Self-Test for CentOS 7 provided with source code (pinout, gateway, PCIe driver & host test application)
Application development	<b>Supported design flows</b> - Quartus Prime Pro (HDL, Verilog, VHDL, etc.)

## Deliverables

- 385A-SoC FPGA board
- Built-In Self-Test (BIST)
- Full and half-height PCI back plates available
- 1-year access to online Developer Site
- 1-year hardware warranty



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