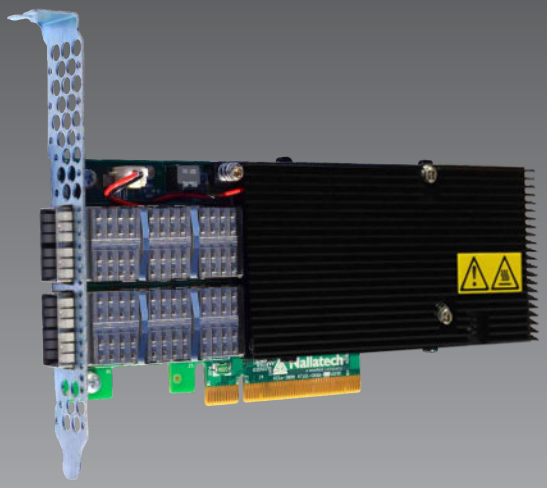
BittWare a molex company

385A
PCIe FPGA Board



Arria 10 Low Profile PCIe FPGA Board

The 385A low profile accelerator card provides a powerful PCIe computing and I/O platform for FPGA development and deployment across a range of application areas including high performance computing, image processing, and network analytics.

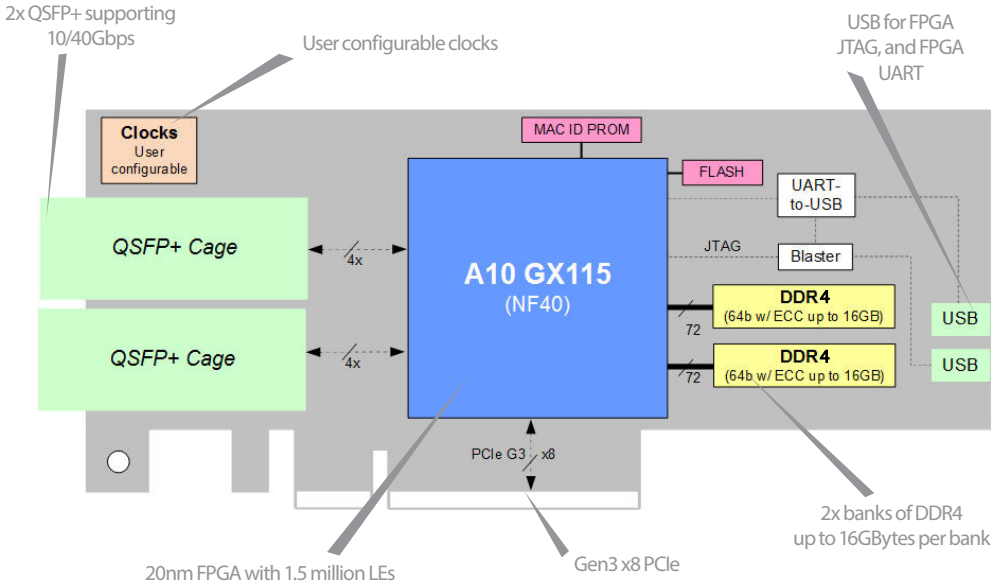
Tool Flow Flexibility for Software- or Hardware-Based Development

- OpenCL support for software-orientated customers
- Abstration for faster development
- Push-button flow for FPGA executable, driver, and API
- Add optimized HDL IP cores to OpenCL designs as libraries

- Traditional VHDL/Verilog support for hardware-orientated customers
- Hand-code for ultimate performance
- High-Level Synthesis (HLS) available for rapid development
- FPGA card designed to support standard Intel IP cores for Stratix 10

key features

Intel Arria 10 GX 1150 | **2x QSFP+ for 10/40Gbps** | **OpenCL BSP**



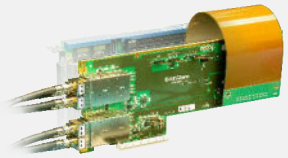
Key Applications

Designed to address a range of compute-intensive and latency-critical applications:

- Compute, Network and Storage
- Finance and Risk Analysis
- Datacenter
- HPC
- Communications (wireless and wireline)
- Industrial, Broadcast, Embedded
- Medical
- Automotive

Additional Services

Take advantage of BittWare's range of design, integration, and support options



Customization

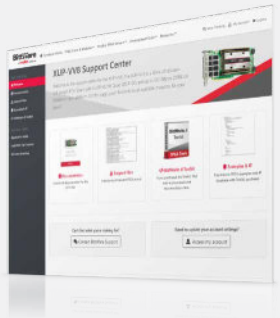
Additional specification options or accessory boards to meet your exact needs.

Server Integration

Available pre-integrated in our TeraBox servers in a range of configurations.

Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

FPGA	• Intel Arria 10 GX
	  • 1150 GX F1517 NF40 package
	  • Core speed grade -2: I/O speed grade -3
	• Contact BittWare for other Arria 10 GX options

On-board Flash	• Flash memory for booting FPGA
On-board memory	• Two banks of DDR4 SDRAM x 72 bits • 4GB per bank (8GB total /16GB and 32GB version also available) • 2133MT/s per bank
Host interface	• x8 Gen3 interface direct to FPGA

QSFP cages	• 2 QSFP+ cages on front panel connected directly to FPGA via 8 transceivers
	• User programmable low jitter clocking supporting 10/40 GbE
	• Each QSFP can be independently clocked
	• Clocking options:
	  • Network recovered with jitter attenuation
	  • QSFP clocking: user programmable, or CPRI, 1GbE
	  • External clock input, 1PPS input

Cooling	• Standard: single-width active heatsink (embedded fan) • Optional: single-width passive heatsink
Electrical	• On-board power derived from 12V PCIe slot • Power dissipation is application dependent • Typical max power consumption 75W
Environmental	• Operating temperature: 5°C to 35°C
Quality	• Manufactured to IPC-A-610 Class 2 • RoHS compliant
Form factor	• Half-height, half-length PCIe single-slot board • 167.6mm x 68.9 mm x 17mm

Development Tools

FPGA development	BIST - Built-In Self-Test for CentOS 7 provided with source code (pinout, gateware, PCIe driver & host test application)
Application development	Supported design flows - Intel FPGA OpenCL SDK, Quartus Prime Pro (HDL, Verilog, VHDL, etc.)

Deliverables

- 385A FPGA board
- USB cable (front panel access)
- Built-In Self-Test (BIST)
- OpenCL HPC Board Support Package (BSP)
- 1-year access to online Developer Site
- 1-year hardware warranty

intel partner Titanium

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