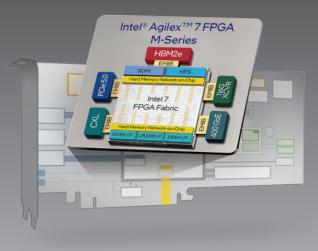
Bittiviare a molex company



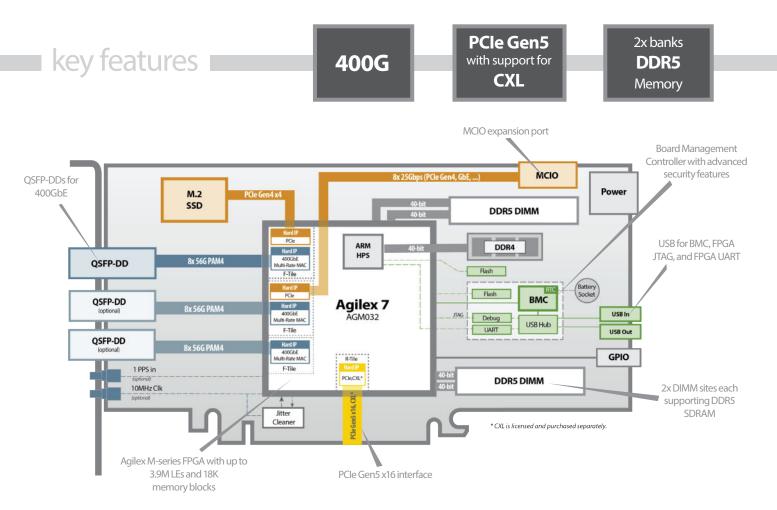


Agilex[™] FPGA card featuring 400G and Gen5 PCle M-series FPGA with DDR5 memory

BittWare's IA-865m is an Intel® Agilex[™] M-series FPGA card optimized for throughputand memory-intensive applications. The M-series FPGA features an extensive memory hierarchy including integrated DDR5 memory interface and a hard memory Networkon-Chip (NoC) to maximize memory bandwidth. The IA-865m card provides a balance of I/O and memory leveraging the Agilex chip's unique tiling architecture with QSFP-DDs, DDR5 SDRAM, M.2 SSD, PCIe Gen5 x16 with CXL support, and MCIO expansion port for a variety of applications.



The IA-865m has support for Intel oneAPI[™], which enables an abstracted development flow for dramatically simplified code re-use across multiple architectures.



Additional Services

Take advantage of BittWare's range of design, integration, and support options



Customization Additional specification options or accessory boards to meet your exact needs.



Server Integration Available pre-integrated in our TeraBox servers in a range of configurations.



IP and Solutions Our portfolio of IP and solutions reduce risk for development and deployment.



Service and Support BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

FPGA	 Intel Agilex 7 M-Series: AGM032 (default) Package: R36A Core speed grade -2; XCVR speed grade -1 CXL with XCVR speed grade -1 (CXL IP is licensed and purchased separately) FPGA includes ARM HPS
ARM HPS	 Dedicated 40-bit DDR4 Dedicated Flash memory for booting ARM Optional 1GbE interface (contact BittWare)
On-board Flash	2Gbit Flash memory for booting FPGA
External memory	 2x 288-pin DDR5 DIMM slots, each supporting 32GB (default) DDR5 SDRAM modules (64GB total)
Host interface	 x16 PCle Gen5 interface direct to FPGA CXL v1.1 (CXL IP is licensed and purchased separately)
M.2 SSD	NVMe PCle M.2 2230 SSD
QSFP-DD cages	 QSFP-DD cage on front panel connected directly to FPGA via 8 transceivers Configuration option for 2x additional QSFP- DDs (contact BittWare) User programmable low jitter clocking supporting 10/25/40/100/400GbE Each QSFP-DD can be independently clocked Jitter cleaner for network recovered clocking Multi-rate hard MAC+FEC Fully backward compatible with QSFP28s
MCIO	x8 connector supporting 2x Gen4 x4 root complexes
External clocking	 1 PPS and 10MHz ref clk front panel inputs (optional)
USB	USB access to BMC, USB-JTAG, USB-UART

Board	 Power sequencing and reset
Management Controller	Voltage, current, temperature monitoring
	Protection shut-down
	Clock configuration
	 Low bandwidth BMC-FPGA comms with SPI link
	• USB 2.0
	PLDM support
	Card-level security
	BMC Root of Trust
	 BMC and FPGA secure boot
	 BMC and FPGA secure upgrade
	Key management
	RTC with battery backup
Cooling	Standard: dual-width passive heatsink
	Optional: dual-width liquid cooling
Electrical	On-board power derived from PCIe slot 12V and
	12-pin AUX power connector
	 Power dissipation is application dependent
	Typical max power consumption TBD
Environmental	Operating temperature: 5°C to 35°C (passive
	heatsink)
Quality	Manufactured to IPC-A-610 Class 2
	RoHS compliant
	CE, FCC and ICES approvals
Form factor	Standard-height, 3/4-length, dual-slot PCIe card
	• 111.15mm x 266.70mm (4.376in x 10.500in)

Development Tools

intel.

AGILEX

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System development	BittWare SDK including PCIe driver, libraries, and board monitoring utilities
Application development	Supported design flows - Intel FPGA oneAPI Base Toolkit, Intel High-Level Synthesis (C/C++) and Quar- tus Prime Pro (HDL, Verilog, VHDL, etc.)

intel

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International Distributors





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